TI-Island-Catalyzed Si Nanowire: Growth on (112) Substrate and Behavior of Its Vertical MOS Structure

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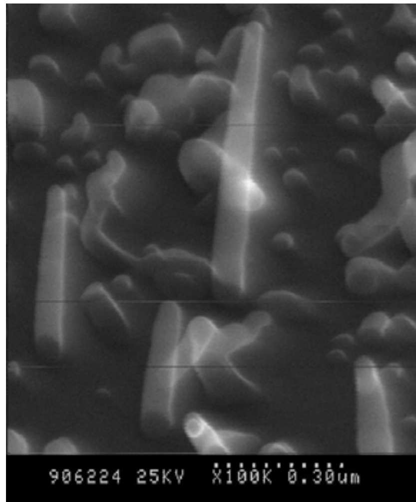
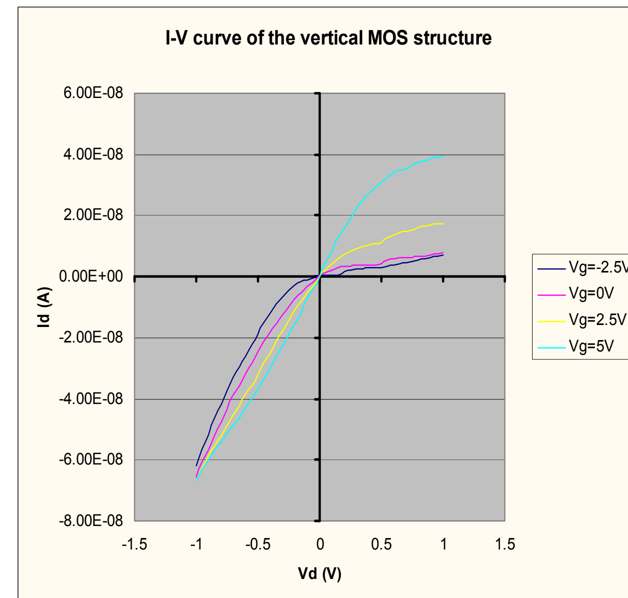
As devices in modern integrated circuits become smaller and smaller, the required sub-100nm feature sizes become difficult and expensive to produce. New nano-scale assembling technology, such as catalyzed nanowires growth and quantum dot growth, may benefit integrated-circuit production by eliminating critical lithography step. Among the metals that have been used for Si nanowire growth, the diffusivity and solubility of Ti in silicon are at least two orders of magnitude lower than that of Au, Fe, Zn, Ni, or Co. Therefore, Ti-catalyzed silicon nanowire is more compatible with integrated-circuit components and applications.

We have grown silicon nanowires catalyzed by Ti islands by molecular beam epitaxy (MBE) using Si_2H_6 as the gas source. Approximately one monolayer of Ti was deposited on Si wafers at 550°C and then annealed above 800°C to form $TiSi_2$ islands. The Si nanowires were then grown at 500°C~600°C by directing a Si_2H_6 molecular beam toward the wafer, with the $TiSi_2$ islands as seeds.



■Si nanowires grown on Si(112) substrate at 570 °C for 60min with 5 sccm Si_2H_6 flow. SEM image at 45°

The silicon nanowires are typically between 20 and 40 nanometers in diameter and several hundred nanometers long. The growth is typically along <112> directions of Si crystal. With (112) Si substrate, Si nanowires perpendicular to the substrate surface are obtained. And the Si nanowires are n-type doped because of the background As flux from the MBE chamber. The wafer is then oxidized at 800°C to form 5nm of native silicon dioxide. Then, in consequence, a layer of 100nm silicon dioxide, a layer of 50nm tungsten as gate, and another layer of 300nm low temperature silicon oxide are deposited. The wafer is then polished down by 200nm and a layer of Ti is deposited as top contact. When applying negative voltage to the aluminum gate layer, the current going through the MOS structure are modulated by field effect.



Measured I-V curves of the vertical MOS structure.