# Noise in Sub100nm Transistors and Nanostructures

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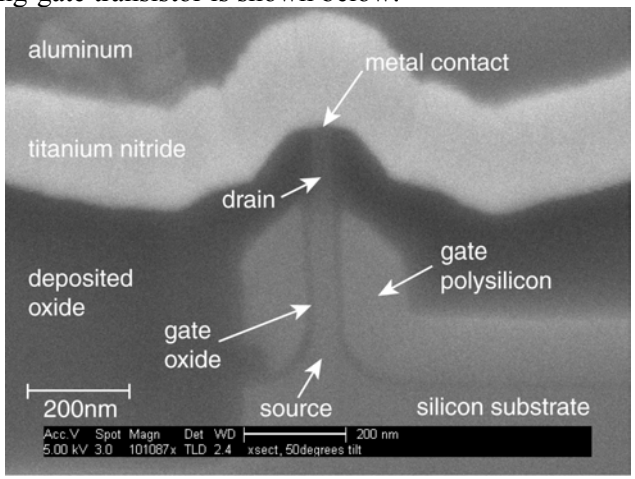
The low frequency noise of bulk MOSFETs has traditionally been much worse than bipolar and JFET devices due to surface 1/f noise caused by capture and release of electrons into oxide traps. As MOSFETs scale into the nano-range, this 1/f contribution to noise figure is expected to become even more significant. Two novel, sub 100nm device structures are fabricated and characterized to explore the lower limits of this noise.

Fully depleted cylindrical surrounding-gate transistors and depletion-mode NMOS transistors are fabricated from silicon nanopillars such that a 100nm long channel is created vertically on the sidewall. Through electron beam lithography and self-limiting oxidation, pillars with silicon cores smaller than 50nm wide are realized. Depletion-mode NMOS transistors are built from elongated fin pillars to achieve measurable drive current even in depletion. The polysilicon surrounding-gate is formed with a spacer process, and final metallization follows passivation and contact hole etches. A cross-section of the cylindrical surrounding-gate transistor is shown below.




The cylindrical surrounding-gate transistor is fabricated with channel area less than 0.02 square microns. At typical trap densities, the average number of traps for this device is expected to be 0.6. Although regions with random telegraph signal noise attributed to a single trap and regions with no random telegraph signal indicating no dominant trap are found, the underlying noise of this device maintains a 1/f spectrum.

The depletion-mode surrounding-gate transistor allows the physical separation of electrons from traps. While the noise far above threshold is found to follow the expected 1/f behavior, near threshold a Lorentzian noise source dominates, as shown below. This excess noise limits the low-noise use of depletion-mode surrounding-gate devices.