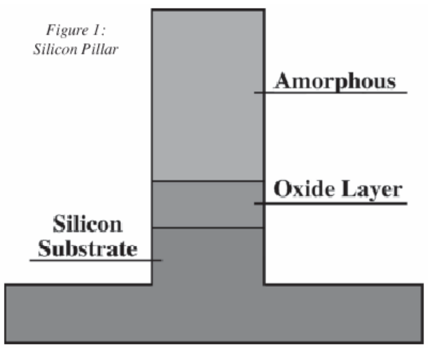
Study of Stress Effects on Crystallization of Amorphous Silicon Pillars

SNF Researcher: Mahmooda Sultana, Chemical Engineering, University of Southern California (2002 SNF REU)
Principal Investigator: James Plummer, Department of Electrical Engineering, Stanford University
Collaborators: Michael Deal, Yaocheng Liu, Department of Electrical Engineering, Stanford University

Crystallization of amorphous silicon at low temperature is a technique that may be used to make 3-D integrated circuits and heterogeneous integration. One of the methods for low-temperature crystallization is to deposit a metal on the amorphous silicon and anneal. The metal forms a silicide and passes along the amorphous silicon layer, allowing the silicon to crystallize at a lower temperature. However, the crystallization yield may vary depending on the amount of stress on the amorphous Si pillars. Nickel has been used in our experiments because nickel reacts with silicon to form nickel disilicide, which has almost the same lattice constant as silicon and produces comparatively better quality of crystal.

Figure 1: Silicon Pillar



In our experiments, the effect of stress on nickel induced crystallization of silicon pillars is studied. Amorphous silicon pillars of different widths are fabricated (Figure 1) and an oxide layer that produces stress on each pillar is deposited around them. The oxide layer is varied for different samples to produce different amounts of stress on the pillars. Nickel is sputtered on the top of the pillars and the samples are annealed at 450C. After annealing, any trace of unreacted nickel from the top and the sides is etched away using aqua regia. The remaining oxide sidewall from each sample is then etched off.

Due to a time constraint and equipment problems, only the three samples with 15 hour anneals have been analyzed for crystallization with TEM (Figure 2). The percentage of crystallization for each combination of pillars is calculated in Figure 3. The graph shows that for small pillars, the percentage of crystallization increases as the oxide thickness decreases. This indicates that crystallization increases as the stress on the pillars decreases. However, as the pillar width increases, there is less effect on crystallization due to varied oxide thickness. In fact, for the largest size (0.4 µm), the oxide thickness seems to have little or no effect on crystallization. This is because, as the size increases, the pillars can better accommodate the stress from the oxide.

For the pillars with the thickest oxide, as the width increases, the percentage of crystallization also increases. That means, as the stress decreases, the percentage of crystallization increases, which is consistent with the result mentioned before for varied oxide thickness. Again, for the oxide-free or stressfree pillars, the size seems to play little or no effect on crystallization, which is similar to that mentioned earlier.

In summary it is observed that pillars with a thinner oxide layer have more crystallization than pillars with a thicker oxide. Also, the crystallization yield is greater for wider pillars that have lesser stress per volume unit than narrower pillars. Therefore, it is found from our experiments that higher compressive stress causes less crystallization. This is important in understanding and optimizing the crystallization process used in fabricating 3-D ICs.

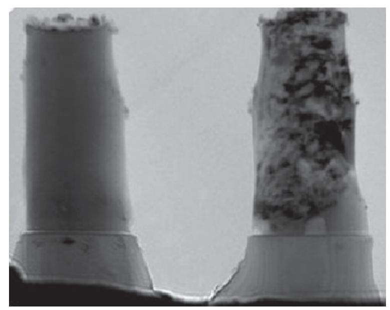


Figure 2: TEM image of pillars (the amorphous pillar is on the left and crystallized pillar is on the right).

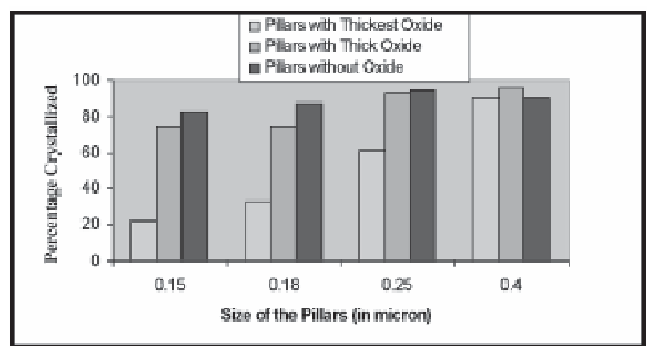


Figure 3: Percentage of crystallization for pillars with different combinations of pillar width and oxide thickness.