

Fabrication of High-Quality p-MOSFET in Ge Grown Heteroepitaxially on Si

Ammar Nayfeh, Chi On Chui, Takao Yonehara, and Krishna C. Saraswat

Abstract—We have successfully demonstrated high-performance p-MOSFETs in germanium grown directly on Si using a novel heteroepitaxial growth technique, which uses multisteps of hydrogen annealing and growth to confine misfit dislocations near the Ge-Si interface, thus not threading to the surface as expected in this 4.2% lattice-mismatched system. We used a low thermal budget process with silicon dioxide on germanium oxynitride (GeO_xN_y) gate dielectric and $\text{Si}_{0.75}\text{Ge}_{0.25}$ gate electrode. Characterization of the device using cross-sectional transmission electron microscopy and atomic force microscopy at different stages of the fabrication illustrates device-quality interfaces that yielded hole effective mobility as high as $250 \text{ cm}^2/\text{Vs}$.

Index Terms—Anneal, dislocations, effective field, effective mobility, germanium, germanium oxynitride (GOI), heteroepitaxy, hydrogen, mobility, MOS devices.

I. INTRODUCTION

GERMANIUM (Ge) has been emerging as a viable candidate to augment silicon for electron device applications [1], [2] due to its superior semiconductor properties as compared to Si. In order to integrate Ge CMOS with Si CMOS for high-performance applications, it is pivotal to develop new methods for heteroepitaxial Ge technology because Ge growth on Si is hampered by the large lattice mismatch (4%). The large mismatch results in growth that is dominated by “islanding” and misfit dislocations that are formed at the Si substrate/Ge film interface terminating at the film surface as threading dislocations, thus degrading device performance. Recently, we demonstrated that the incorporation of hydrogen annealing in the growth recipe reduces the Ge diffusion barrier, dramatically improving the surface roughness [3].

To date, heteroepitaxial Ge-based electron devices have focused more so on photodetectors [4], [5] with only a few publications on MOS transistors that required an Si cap layer [6], [7] or a graded SiGe buffer layer in between Ge and Si [8]. Bojarczuk *et al.* recently showed epitaxial growth of Ge on a crystalline oxide, $\text{La}_x\text{Y}_y\text{O}$, that requires an Si surfactant layer during the growth recipe [9]. In this paper, we report on

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the fabrication and demonstration of high-quality Ge-based p-MOSFETs using a recently developed procedure [10], multiple hydrogen annealing for heteroepitaxy (MHAH), that employs multiple cycles of growth and hydrogen anneal, for growing high-quality thick heteroepitaxial Ge layers on silicon.

II. HETEROEPITAXIAL GROWTH

We begin the process with standard bulk silicon wafers with resistivity of 1–5 $\Omega\text{-cm}$. The wafers were dipped in 50:1 $\text{H}_2\text{O}:\text{HF}$ (hydrofluoric acid) for 30 s and immediately loaded in an ASM Epsilon-II epitaxial reactor. A hydrogen bake at 950°C was carried out to insure that no native oxide remained on the surface. In the first step, a Ge layer was grown at 400°C at a reduced pressure of 10 torr. This was followed by a hydrogen anneal for 1 h at 825°C and at a pressure of 80 torr, which yielded $\sim 155 \text{ nm}$ of Ge with rms surface roughness of 2.9 nm [3]. In the second step, we deposited an additional 250 nm of Ge using the above growth conditions, followed by additional hydrogen anneal at 700°C and 80 torr, which yielded 400 nm of Ge.

III. p-MOS FABRICATION

Using a $\sim 400\text{-nm}$ high-quality MHAH-grown Ge layer on Si as the starting substrate with *in situ* substrate doping of $1 \times 10^{17} \text{ cm}^{-3}$ n-type, p-MOS transistors were fabricated. Field isolation was done in a rapid thermal processing (RTP) system using ammonia to grow to a thin GeO_xN_y (8 nm) [11] layer at 600°C followed by LPCVD SiO_2 (LTO) deposition (400 nm). After active area opening, 8-nm GeO_xN_y was grown using the RTP system at 600°C followed by 10-nm LTO deposition at 450°C as the gate dielectric yielding 14-nm equivalent oxide thickness (EOT). Immediately following the LTO deposition, an *in situ* boron-doped $\text{Si}_{0.75}\text{Ge}_{0.25}$ gate was grown by CVD at 500°C . After gate definition and self-aligned source/drain boron (B) implant, a 450°C rapid thermal anneal (RTA) was used to activate the dopant. Contacts were defined by LTO/aluminum and a 400°C forming gas anneal concluded the process.

IV. RESULTS AND DISCUSSION

The characteristic quality of the interface at different stages of the fabrication and the analysis of the device operation are described. After the first growth and anneal, the surface roughness is reduced by 90% due to reduction in the Ge-H diffusion barrier. Additionally misfit dislocations terminate away from the top surface. Fig. 1(a) is a cross-sectional TEM image of the $\sim 155 \text{ nm}$ of Ge grown on Si, showing that misfit dislocations terminate below the surface. Also, it was shown earlier [3] that

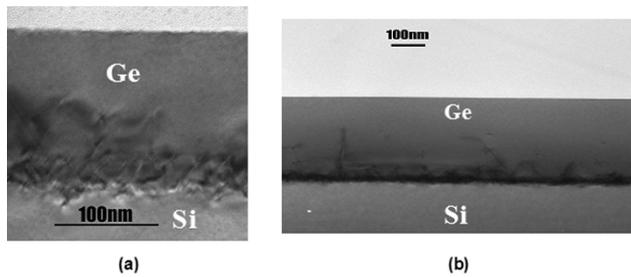


Fig. 1. Cross-sectional TEM image of (a) ~ 155 nm heteroepitaxial-Ge layer on Si grown with a single growth and H_2 anneal step and (b) ~ 400 -nm heteroepitaxial-Ge layer on Si grown by the MHAH method: (i) Ge-growth (both): 400°C and 10 torr, (ii) H_2 bake 1: 80 torr at 825°C for 1 h, and (iii) H_2 bake 2: 700°C for 1 h. Misfit dislocations are confined to the Ge/Si interface, leaving a high-quality top Ge layer.

MOS capacitors fabricated using this procedure and GeO_xN_y gate dielectric exhibit good C_g - V_g characteristics with negligible hysteresis. This indicated that the first hydrogen anneal not only improves the surface roughness but also the quality of the layer. We believe [10], during the hydrogen annealing, that Si diffusion from the substrate into the growing Ge layer enhances the mechanism for Ge to relax as confirmed by X-ray diffraction (XRD), and thus subsequent growth is homoepitaxy of Ge on Si with the final ~ 400 -nm layer being 96% Ge deduced from Rutherford back scattering (RBS) measurements. Fig. 1(b) is a cross-sectional TEM image of ~ 400 nm of Ge grown on Si using the MHAH method, showing that misfit dislocations are confined or bent parallel to the Si/Ge interface leaving a high-quality Ge layer. Then, $10 \times 10 \mu\text{m}^2$ AFM scans of the surface yielded a final surface roughness of 2.9 nm compared to 24 nm from Ge grown directly on Si, making the layer suitable for subsequent gate dielectric growth.

Fig. 2(a) and (b) presents the I - V characteristics of the p-MOSFETs. In Fig. 2(a), we present the I_s - V_s curves, while I_d - V_d is shown in Fig. 2(b). W/L of this device is $100 \mu\text{m}/6 \mu\text{m}$. In the measurement, V_d was swept from 0 to -1 V and V_g was stepped in 0.1-V increments from 0 to 1.6 V, while V_s and V_{sub} were grounded. Comparing the I_d - V_d and I_s - V_s curves, one can observe a small asymmetry originating at the drain side, which implies leakage current. Fig. 2(c) shows the substrate (I_{sub}) and gate (I_{gate}) current as a function of drain voltage. As drain voltage increases, the substrate current increases while the gate leakage decreases and is less than $6 \times 10^{-6} \mu\text{A}/\mu\text{m}$. I_{sub} is independent of V_g while I_g is a strong function of V_g as expected. As a result, the leakage current seen on the drain side is largely due to drain-to-substrate leakage resulting from either or a combination of junction leakage due to a small Ge bandgap or from electrostatic interaction between the drain depletion region and confined defect region. In fact, one would expect the latter leakage path based on analytic calculations of the drain depletion width and thickness of the epi-Ge layer. Thicker Ge layers could help alleviate this leakage problem and help quantify more the junction leakage. The high-quality Ge layer will be used to fabricate of germanium-on-insulator (GOI) substrates using epitaxial Ge by bonding and layer transfer [12].

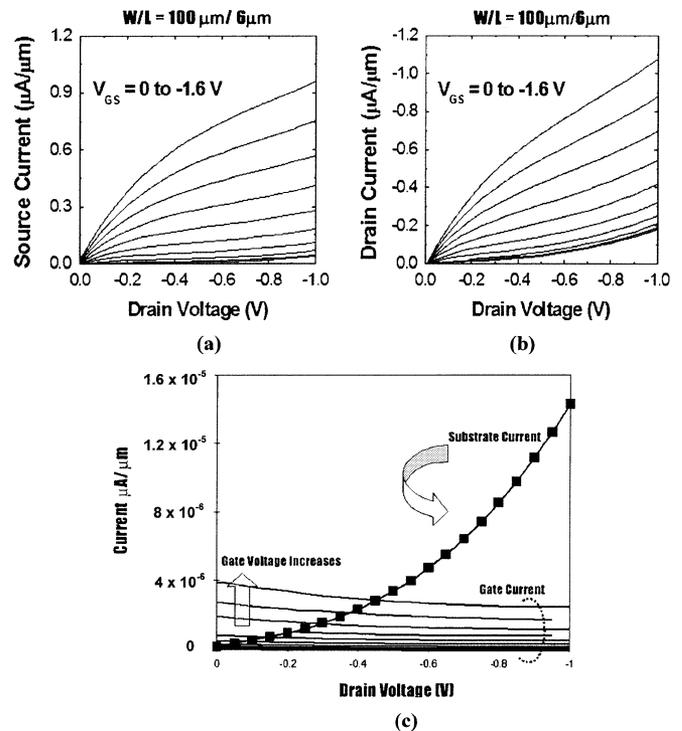


Fig. 2. Measured (a) I_s - V_s , (b) I_d - V_d characteristics, and (c) $I_{\text{sub}}/I_{\text{gate}}$ - V_d characteristics; I_{sub} is independent of V_g .

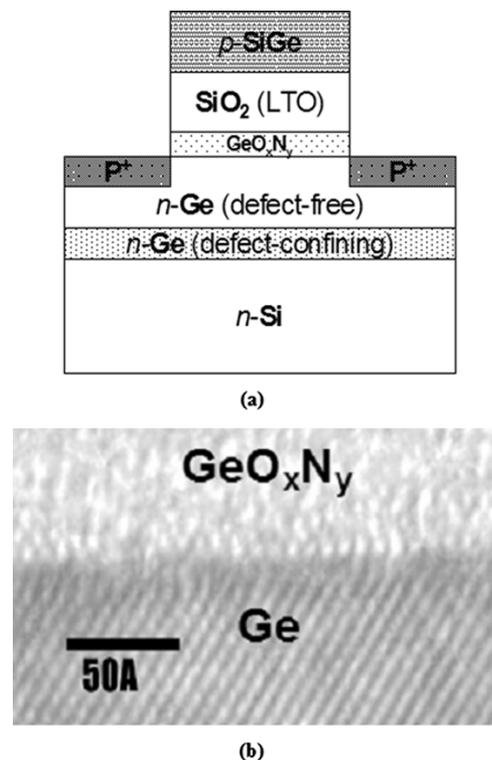


Fig. 3. (a) Cross section of p-MOSFET fabricated using $\text{Si}_{0.75}\text{Ge}_{0.25}$ gate electrode and LTO/ GeO_xN_y gate dielectric. Channel region is high-quality single-crystal Ge. (b) High-resolution cross-sectional TEM of GeO_xN_y /Ge stack showing the Ge single-crystal lattice and high-quality interface.

Effective mobility μ_{eff} was extracted using the simple I_d - V_d method according to

$$\mu_{\text{eff}} = \left(\frac{2L}{W} \right) \times I_d \times \frac{1}{C_{\text{ox}}(V_g - V_t)}. \quad (1)$$

Threshold voltage V_t was extracted to be 0.7 V from I_d - V_g slope extrapolation. The V_t shift on this p-MOS device is due to the p-type SiGe-doped gate electrode. Effective mobility (μ_{eff}) was calculated at two points to be $\sim 250 \text{ cm}^2/\text{V}\cdot\text{s}$ at $V_g - V_t = 80 \text{ mV}$ and $\sim 95 \text{ cm}^2/\text{V}\cdot\text{s}$ at $V_g - V_t = 1 \text{ V}$, which corresponds to low and high overdrive, respectively. We should note that this procedure overestimates the amount of charge in the channel and thus gives underestimates for mobility. The effective field can be calculated for holes using

$$E_{\text{eff}} = \frac{1}{\epsilon_{\text{Ge}}} \left(|Q_d| + \frac{1}{3}|Q_i| \right) \quad (2)$$

from Gauss's law, where Q_d is the depletion charge and Q_i is the inversion charge. This equation can be simplified using $\epsilon_{\text{Ge}} \approx 4\epsilon_{\text{ox}}$ with

$$|Q_d| = C_{\text{ox}}(V_t - V_{\text{fb}} - 2\psi_B) \quad (3)$$

and

$$|Q_i| \approx C_{\text{ox}}(V_g - V_t) \quad (4)$$

to

$$E_{\text{eff}} = \frac{V_t - V_{\text{fb}} - 2\psi_B}{4t_{\text{ox}}} + \frac{V_g - V_t}{12t_{\text{ox}}}. \quad (5)$$

Ψ_B is the separation of the Fermi level from the midgap in the Ge, and V_{fb} is the flatband voltage [13]. Using the work function of the heavily doped SiGe gate and doping concentration of the Ge, we calculated using (5) that $V_g - V_t = 80 \text{ mV}$ corresponds to the effective field of 0.15 MV/cm and $V_g - V_t = 1 \text{ V}$ to 0.21 MV/cm. From the universal mobility curves for silicon, the effective field of 0.15 MV/cm corresponds to effective mobility of approximately $\sim 125 \text{ cm}^2/\text{V}\cdot\text{s}$ while the effective field of 0.21 MV/cm corresponds to the effective mobility of approximately $\sim 31 \text{ cm}^2/\text{V}\cdot\text{s}$ [14]. Thus, the epi-Ge devices show a $2\times$ enhancement in effective mobility at a low effective field and a $3\times$ enhancement at a high effective field. The high effective mobility indicates the high quality of the CVD-grown heteroepitaxial Ge channel. Fig. 3(a) is a schematic cross section of the final device fabricated while Fig. 3(b) is a high-resolution cross-sectional TEM image showing the high-quality GeO_xN_y /epi-Ge interface and the Ge single crystal atomic lattice.

V. CONCLUSION

We have successfully demonstrated high-mobility Ge-based p-MOSFETs in germanium grown directly on Si using a novel technique that allows growth of high-quality thick heteroepitaxial-Ge layers on Si. Misfit dislocations that are expected to thread to the surface remain confined near the Ge/Si interface or bend parallel to the surface.

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