



Low Temperature Germanium Growth on Silicon Oxide Using Boron Seed Layer and In Situ Dopant Activation

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Low temperature (<350°C) growth of germanium (Ge) on silicon dioxide (SiO₂) is demonstrated using a diborane pretreatment technique. Using SiH₄ and B₂H₆ precursors, Si_{1-x}B_x layers are deposited on SiO₂ to seed the chemical vapor deposition growth of Ge films. In the SiH₄:B₂H₆ system, the binary deposition mechanism of the Si_{1-x}B_x film is explained by the “enhancement” model. In situ doping of Ge films is also investigated. In situ boron activation is achieved during the crystallization of the Ge films at 310°C. Device applicability of the doped Ge film growth on oxide is demonstrated in a low temperature (350°C) Si p-channel metal-oxide-semiconductor field-effect transistor, in which the Ge layer is used as a gate electrode. The low temperature Ge growth technique can be used for low thermal budget processes, e.g., monolithic three-dimensional integrated circuits. © 2010 The Electrochemical Society. [DOI: 10.1149/1.3295703] All rights reserved.

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Complementary metal oxide semiconductor scaling has led to the high performance and low power operation of ultralarge-scale integration devices.¹⁻³ However, scaling transistors to the nanometer regime is plagued with many challenges, including gate leakage, mobility degradation, reliability issues, and increasing vulnerability to random process variations. Recently, 45 nm node devices comprising high-*k*/metal gate and strained-channel technologies have been commercially produced.⁴ However, due to growing standby power consumption as a consequence of device shrinking, further scaling is experiencing serious roadblocks. Soon, scaling will certainly face physical limits, requiring a paradigm shift to monolithic three-dimensional (3D) integrated circuits (ICs).^{5,6}

Monolithic 3D-IC technology has several benefits compared to other approaches, e.g., wafer-to-wafer, chip-to-wafer, and chip-to-chip bonding. Monolithic 3D-IC provides increased logic density without a serious 3D wafer-to-wafer alignment problem as well as complicated, deep via fabrication. In addition, the monolithic approach is free from the yield degradation problem, which plagues the device wafer stacking method. While promising for future technologies, monolithic 3D-IC fabrication is still challenging. Devices must be fabricated above copper interconnects that incorporate fragile, porous, low dielectric constant materials.^{7,8} To realize the monolithic 3D-IC, high quality Si and Ge channels and low temperature process technologies for gate oxide, gate electrode, and source/drain (S/D) are required. To grow Ge films on SiO₂ without damaging the material layers underneath, a low temperature low pressure chemical vapor deposition (LPCVD) technique is desired. Conventionally, an LPCVD Si layer deposited at 500°C is used as a seed for Ge growth on SiO₂.⁹ However, this approach is not applicable to the monolithic 3D-ICs. Low temperature processes (<350°C) are thus required to preserve the underlying interconnects and devices.

In this paper, we focus on low temperature Ge growth on silicon dioxide and low temperature Ge process technologies as vehicles for realizing monolithic 3D-ICs. We have developed a low temperature LPCVD Ge growth technique using a seed approach, which is potentially useful for low resistance gate electrodes as well as high mobility channels.¹⁰ Specifically for the gate electrode application, the Ge layer formed by conformal LPCVD can be used for 3D channel structures, such as double-gate and Fin-type transistors. The applicability of our doped LPCVD Ge film process has been demonstrated in Si p-channel metal-oxide-semiconductor field-effect

transistors (PMOSFETs) using a fully low temperature plasma gate oxide¹¹ and Schottky S/D technologies for monolithic 3D-ICs.

Experimental

The starting substrates were Si wafers (n-type, 5–10 Ω cm) with 200 nm silicon dioxide (SiO₂) grown by wet thermal oxidation. The wafers were cleaned in 4:1 H₂SO₄:H₂O₂ at 90°C for 10 min and 5:1:1 H₂O:HCl:H₂O₂ at 70°C for 10 min, followed by deionized water rinse and N₂ drying. The Ge film was deposited in an LPCVD epi chamber (Applied Materials Epi Centura) using a pure GeH₄ precursor. Hydrogen (6 slpm) was used as a carrier gas. Before the Ge deposition, a boron-based pretreatment was used to prepare the wafer surface at 350°C for 1 min. This pretreatment was done using a diborane (B₂H₆) precursor diluted to 1% by hydrogen in some cases and B₂H₆/SiH₄ mixture gas for other samples. The substrate temperature was then changed to 310°C to grow a germanium film on SiO₂ using GeH₄ precursor. In situ doped p- and n-type Ge films were grown by using B₂H₆ and PH₃ precursors, respectively, during the Ge film growth. Dopant activations was done at temperatures below 350°C.

Si PMOSFETs using the in situ boron-doped Ge gate electrode process were integrated with a radical oxidizing gate dielectric and Schottky Pt silicide S/D at temperatures below 350°C. The starting substrates were Si wafers (n-type, 5–10 Ω cm), which were cleaned in 4:1 H₂SO₄:H₂O₂ at 90°C for 10 min and 5:1:1 H₂O:HCl:H₂O₂ at 70°C for 10 min, followed by deionized water rinse and N₂ drying. A plasma oxidation technique¹² was used to form the low temperature gate oxide. Specifically an 8.3 nm gate oxide was formed using a slot plane antenna (SPA) plasma system with 3.4 kW and 2.45 GHz microwave under 50 mTorr, O₂/Ar chemistry at 350°C (Tokyo Electron Trias).¹³ After gate oxide formation, the in situ boron-doped Ge films were deposited on the oxide using various pretreatment conditions. A thin low temperature oxide (LTO) film was subsequently deposited as a cover layer to enhance photoresist adhesion. The Ge film and most of the plasma SiO₂ dielectric were dry-etched to form the gate electrode. After removing the LTO layer and the remaining SiO₂ on the top of the S/D regions by using 2% HF, 5 nm Pt was deposited using a metal evaporator. The prepared samples were annealed at 350°C for 1 h to form a silicide in the source and drain regions.

The film thickness of the deposited Ge on SiO₂ was determined by secondary electron microscopy (SEM). Surface roughness of the Ge films was measured by atomic force microscopy (AFM). X-ray photoelectron spectroscopy (XPS) was used to analyze the surface composition of SiO₂ after the pretreatment and to detect dopants in the in situ doped Ge film deposition. Ge film crystallization was examined by X-ray diffraction (XRD) (Cu Kα, λ = 1.5408 Å).

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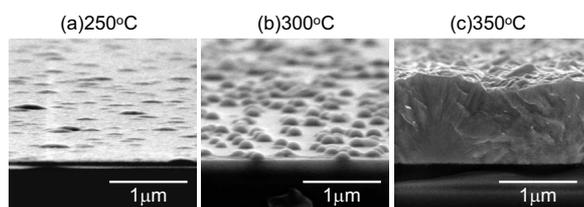


Figure 1. SEM images of poly-Ge films on SiO₂ substrate using LPCVD GeH₄ at (a) 250, (b) 300, and (c) 350°C without seed layers.

Results and Discussion

Deposition of Ge film using low temperature seed layer.— To grow Ge films on SiO₂ without damaging underlying devices, a low temperature LPCVD technique is desired. Conventionally, an LPCVD Si layer deposited at 500°C has been used as a seed for Ge growth on SiO₂. However, this approach is not applicable for monolithic 3D-IC fabrication. Figure 1 presents SEM images of the Ge

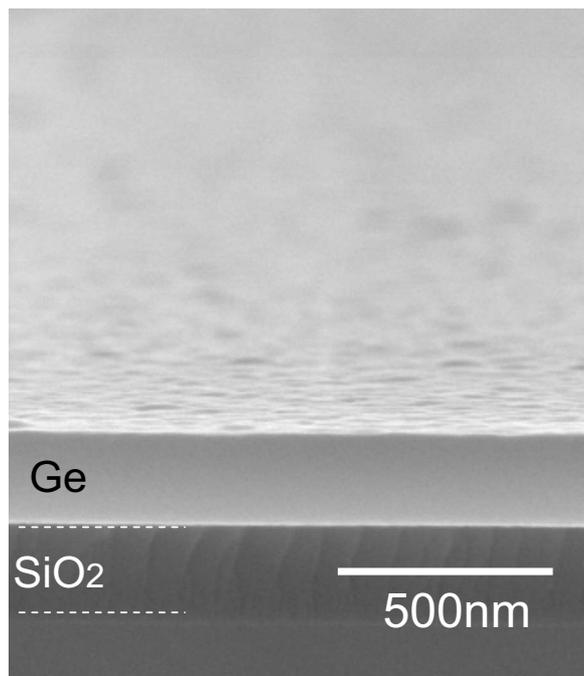


Figure 2. SEM image of poly-Ge films on SiO₂ substrate using LPCVD GeH₄ at 310°C with the diborane pretreatment.

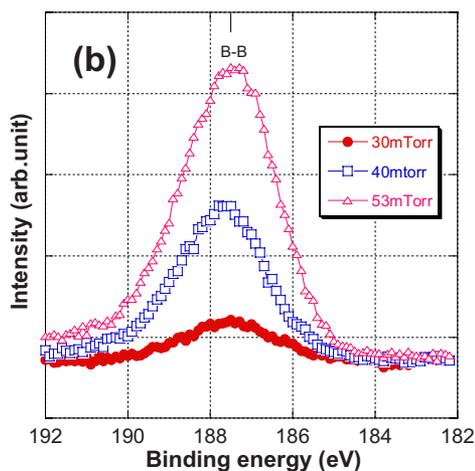
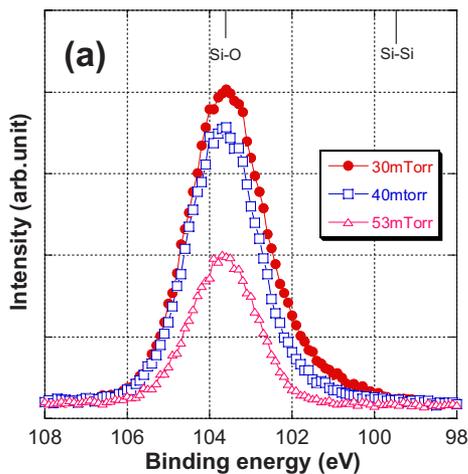


Figure 3. (Color online) XPS analysis of the SiO₂ surface after diborane pretreatment at various partial pressures of diborane. (a) Si 2p and (b) B 1s.

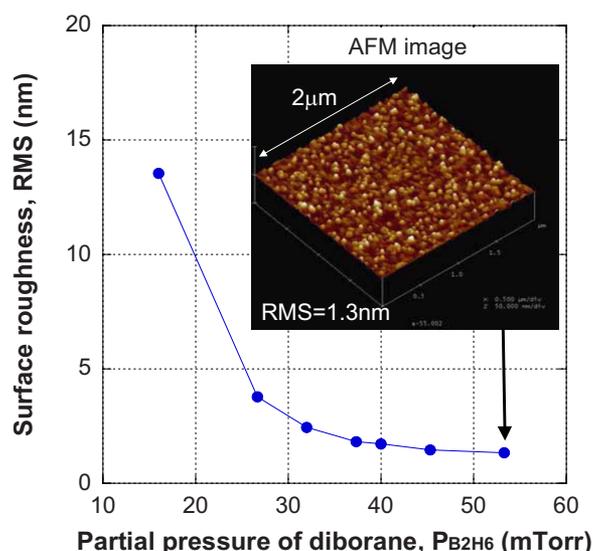


Figure 4. (Color online) Surface roughness (root-mean-square) of Ge film on SiO₂ as a function of the diborane partial pressure in the pretreatment step.

films on SiO₂ without pretreatment. The Ge deposition shows poor nucleation density on SiO₂ at temperatures below 350°C and higher growth rates above 350°C. Therefore, it is difficult to obtain a uniform Ge film on SiO₂ without a seed layer. To obtain a smooth Ge film surface on SiO₂, the nucleation density should be increased while keeping the growth rate low. We use a boron-based layer as the seed to increase the nucleation density. Moreover, the temperature of the film growth is kept low at 310°C to suppress the abrupt growth.

Figure 2 shows SEM images of the Ge film on SiO₂ with the diborane pretreatment. A uniform and continuous Ge film is obtained due to the high nucleation density on SiO₂. Figure 3 shows the XPS spectra of (a) Si 2p and (b) B 1s after the pretreatment step at various diborane partial pressures. The substrate temperature is kept at 350°C, and the duration of the diborane exposure is fixed at 1 min. From the surface analysis, boron is detected on the surface of the substrate SiO₂. Weaker B–H bonds of B₂H₆ (35 kJ/mol) compared to the Si–H bonds of SiH₄ (323 kJ/mol) promote attachment of boron atoms on the SiO₂ surface, which increases Ge grown nucleation. By increasing the partial pressure of diborane in the pretreatment step, the peak intensity is increased, indicating the higher deposition rate of the boron layer. Figure 4 shows the surface

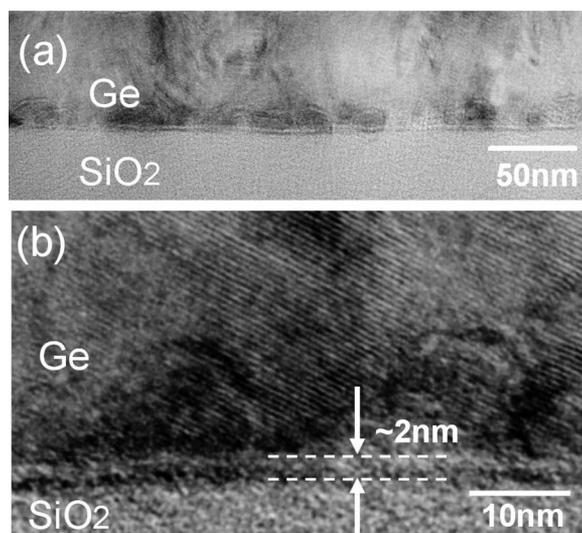


Figure 5. Bright-field TEM images of cross section of poly-Ge film deposited at 310°C after the diborane pretreatment, $P_{B_2H_6} = 40$ mTorr at 350°C. (a) Low and (b) high magnification.

roughness of the Ge film as a function of the partial pressure of diborane in the pretreatment step. The surface roughness of the Ge film was reduced by increasing the diborane partial pressure. Uniform growth of the boron-rich layer on SiO_2 is needed to reduce the surface roughness of the Ge film. Figure 5 shows the transmission electron microscopy (TEM) images of a Ge film deposited after a

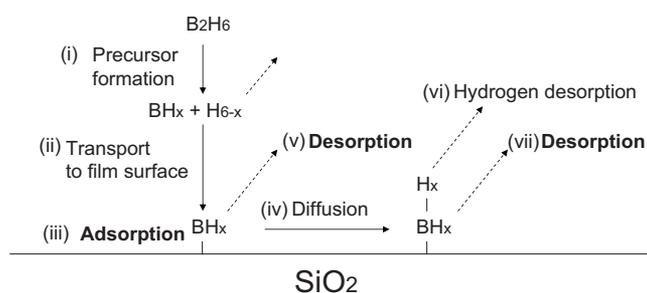


Figure 6. Schematic model describing important steps in deposition of boron.

diborane pretreatment of 40 mTorr for 1 min [(a) low magnification and (b) high magnification]. A 2 nm thick boron layer is apparent between Ge and SiO_2 .

Growth of low temperature seed layers.—Figure 6 shows a schematic model describing the sequence in the deposition of the boron seed film. First, the diborane gas is thermally initiated as a precursor and transported to the SiO_2 surface: (i) A small binding energy of B–H (35 kJ/mol) enhances the BH_x precursor formation at 350°C, a temperature lower than that used for conventional Si seed deposition. [(ii) and (iii)] Second, the initiated precursors are adsorbed on the surface. (iv) Once on the surface, they diffuse until they eventually find a stable site (v) or are desorbed. (vi) The hydrogen must be desorbed to complete the deposition step and yield new nucleation sites.¹⁴ Here, the deposition of boron atoms is defined as the total of the (iii) adsorption and [(v) and (vii)] desorption. A higher partial pressure of the diborane gas increases the probabilities of (i) precursor formation and (iii) adsorption, resulting in higher deposition rates. The sequence of (i) and (iii) is limited by the supply of diborane.

As an alternative, B_2H_6/SiH_4 mixture gas is also demonstrated for seed layer growth. By adding diborane to SiH_4 , a $Si_{1-x}B_x$ film is deposited on SiO_2 as a seed layer for the Ge deposition. Figure 7 shows (a) silicon fraction and (b) deposition rate of the $Si_{1-x}B_x$ film as a function of the diborane gas fraction ratio in the mixture. The total pressure of the chamber is fixed at 160 Torr. The silicon fraction in the film is analyzed by XPS, while the film thickness is measured by SEM and TEM. The addition of diborane to SiH_4 enhances the decomposition of SiH_4 at a low temperature of 350°C, resulting in the growth of $Si_{1-x}B_x$ on SiO_2 . Film composition can be tuned via the diborane ratio. For a diborane flow ratio below 0.025%, boron is not detected by XPS, indicating that the boron concentration in the film is below 1%. For the LPCVD seed layer application, gas chemistries of pure diborane or low concentration diborane (below 10^{-4}) with SiH_4 are desirable to maintain a small seed deposition rate. We apply the enhancement model¹⁵ to explain the relationship between the source gas ratio and the film composition. The boron fraction of the $Si_{1-x}B_x$ film is enhanced by a constant factor, J . This behavior can be described by the following equation

$$\frac{x}{1-x} = J \frac{P_{B_2H_6}}{P_{SiH_4}} \quad [1]$$

where J is the enhancement factor and x is the boron atomic film fraction. $P_{B_2H_6}$ and P_{SiH_4} are the respective partial pressures of SiH_4

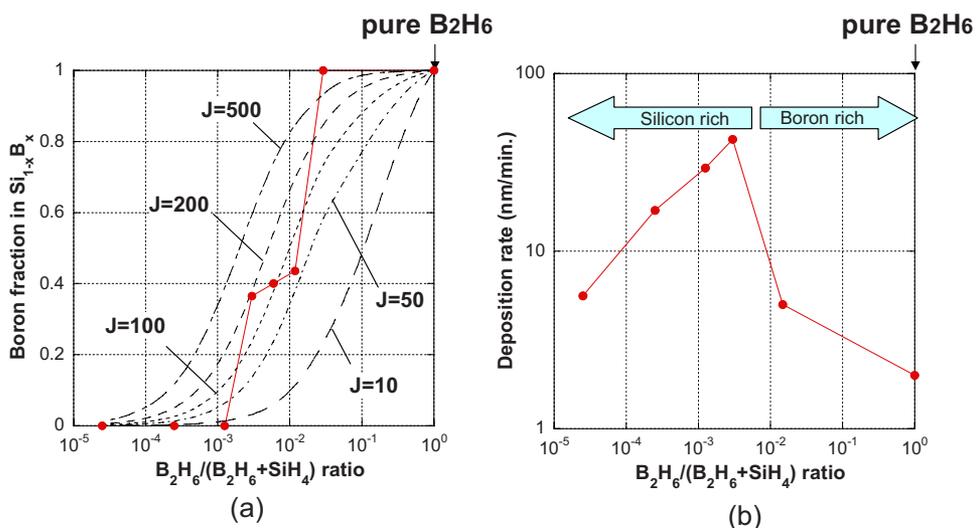


Figure 7. (Color online) (a) Silicon fraction in the film and (b) deposition rate as a function of diborane ratio in the source gas.

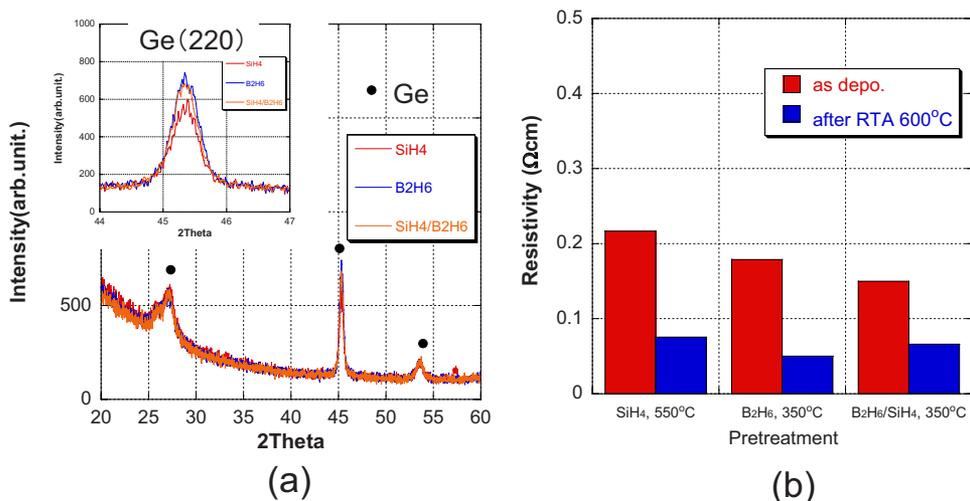


Figure 8. (Color online) (a) XRD patterns of poly-Ge films and (b) film resistivity of undoped Ge films using different pretreatment.

and B₂H₆ in the deposition system. Equation 1 can be written in a fractional form

$$x = \frac{Jf}{(1-f) + Jf} \quad [2]$$

where f is defined as the B₂H₆ fraction of the source gases

$$f = \frac{P_{B_2H_6}}{P_{SiH_4} + P_{B_2H_6}} \quad [3]$$

In this simple assumption, the J factor does not depend on the ratio of the source gases and is estimated to be 60–200 in the SiH₄/B₂H₆ system, indicating that the boron fraction of the film is higher than the B₂H₆ fraction in the source gas mixture.

Next, we compare the effect of the three kinds of pretreatment on the Ge film growth, (a) SiH₄ treatment at 550°C as a reference, (b) B₂H₆ treatment at 350°C, and (c) B₂H₆/SiH₄ mixture treatment at 350°C. Figure 8a shows the XRD profiles of the undoped Ge films using the various pretreatments. All peaks are identified as cubic germanium, and the profiles do not depend on the pretreatment specifics. Apparently, all Ge film samples are strongly oriented in (220). Figure 8b shows the resistivity of the undoped Ge film as deposited and after rapid thermal annealing (RTA) at 600°C for 1 min. It is assumed that the conductive nature of the undoped Ge film is due to the grain boundaries. The RTA process improves the crystallinity of the undoped Ge film. The higher crystallinity leads to a higher mobility, resulting in a lower film resistivity. Across the various seed layers, almost the same film resistivity is obtained, indicating that the seeds are stable during the thermal treatment. For the following experiments, we select the diborane pretreatment for seed layer deposition.

In situ dopants activation in Ge.— B₂H₆ and PH₃ precursors are mixed with GeH₄ for in situ p- and n-type doping, respectively.

Figure 9 shows (a) film resistivity, (b) Ge(111) intensity of the film by XRD measurement, and (c) deposition rate. By increasing the diborane flow ratio, the resistivity of the poly-Ge film decreases, and a significantly low resistivity of ~1 mΩ cm is obtained with a 0.2 diborane ratio at 310°C with no additional thermal treatment. This result indicates that boron is in situ activated during Ge deposition at 310°C. The crystallinity of Ge(111) and the deposition rate also depend on the diborane flow ratio, with excess doping of boron resulting in an amorphous phase and reducing the deposition rate. The boron-induced amorphization of the Ge film degrades not only boron activation but also carrier mobility, resulting in a high resistivity. In contrast, phosphorus is not sufficiently activated at 310°C due to poor crystallization. Rather, a higher temperature (> 350°C) is needed for activating phosphorus. Phosphorus acts as an acceptor at 350°C. A small addition of phosphine into the mixture gas increases the film resistivity due to the p-type background, in which grain boundaries have an n-type character (see Fig. 8b). Therefore, the addition of phosphorus compensates the film, resulting in a higher resistivity. Further addition of phosphine reduces the resistivity because the phosphorus acts as an acceptor. Excess doping of phosphorus changes the Ge phase to amorphous, in which the dopants are not activated. The appropriate doping of boron and phosphorus accelerates the deposition rate and improves film crystallinity. We selected the heavily boron-doped Ge film (~1 mΩ cm) for a p-type gate electrode to demonstrate the in situ dopant activation for a fully low temperature transistor technology.

Demonstration of the Ge film for gate electrode in Si PMOSFET.— Si PMOS transistors using the in situ boron activated Ge gate electrode were integrated with a radical oxidizing gate dielectric and Pt silicide¹⁶ S/D at temperatures below 350°C. Figure 10 shows a cross-sectional schematic image of the low temperature processed Si PMOSFET. In this work, we used the Si substrate as a channel to study the feasibility of the low temperature processes.

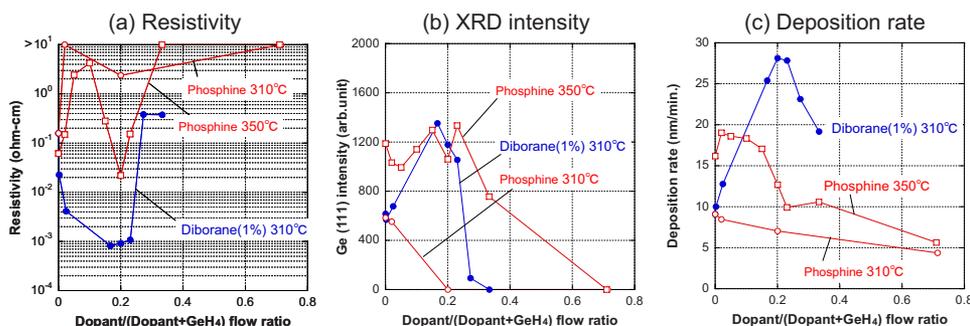


Figure 9. (Color online) (a) Resistivity of doped Ge films as a function of dopants flow ratio. Diborane (1%, diluted by hydrogen) and phosphine are used for the dopant sources. (b) Ge(111) peak intensities by XRD 2θ-θ measurement as a function of dopants flow ratio. (c) Deposition rate of the doped Ge films as a function of dopants flow ratio.

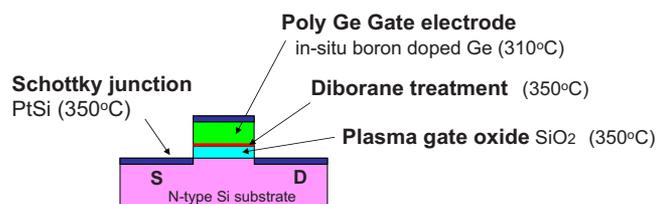


Figure 10. (Color online) Cross-sectional schematic image of the low temperature processed Si PMOSFET.

The diborane pretreatment time is fixed at 1 min, and the partial pressure is 40 mTorr. In the Ge growth step, the diborane flow ratio is kept at 0.2.

Figure 11 shows the capacitance–voltage (C - V) curves of a boron-doped poly-Ge gate capacitor with the diborane pretreatment measured at 1 kHz. Clear C - V curves with no hysteresis are obtained. The extracted equivalent oxide thickness in accumulation is almost the same as that in inversion, indicating that the Ge electrode acts as a metal due to the heavy boron doping.

Figure 12 shows characteristics of a Si PMOSFET integrated by

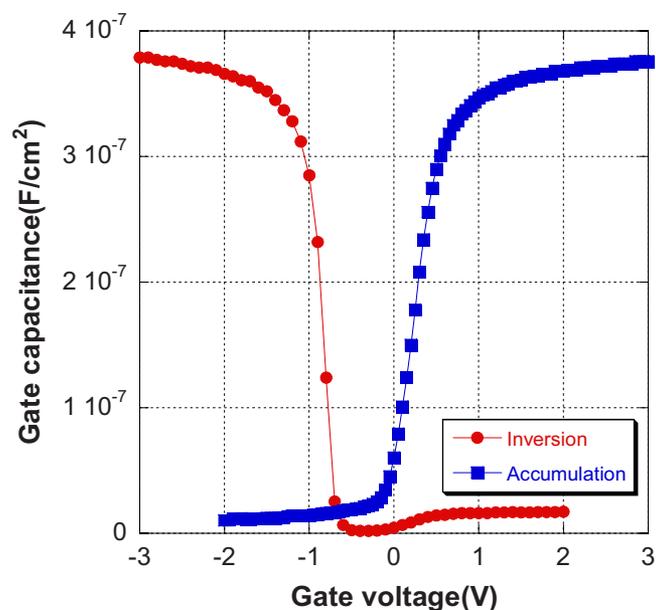


Figure 11. (Color online) C - V curves of boron-doped poly-Ge gated capacitor with the diborane pretreatment of 40 mTorr, measured at 1 kHz.

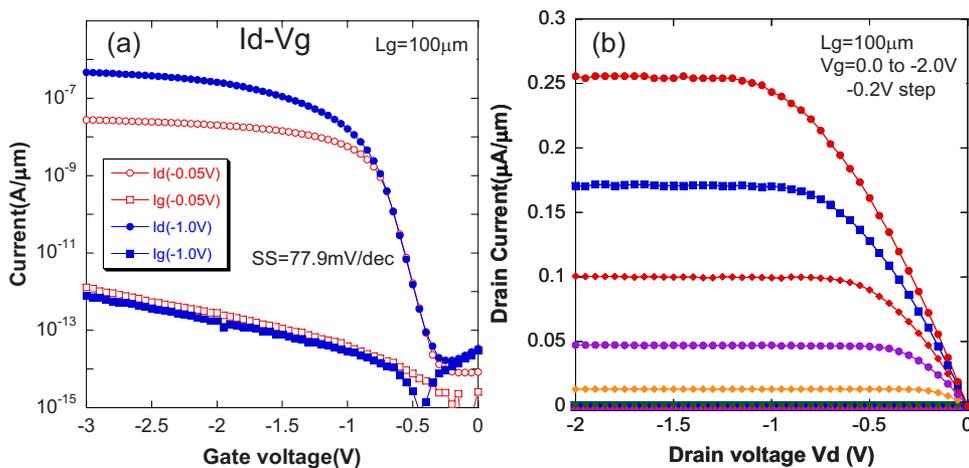


Figure 12. (Color online) (a) I_d - V_g curves of the Si PMOSFET with 200 nm poly-Ge gate electrode, PtSi S/D and 8.3 nm SPA gate oxide (350°C), measured at $V_d = -0.05$ and -1.0 V. (b) I_d - V_d characteristics of the Si PMOSFET formed by the fully low temperature transistor technology.

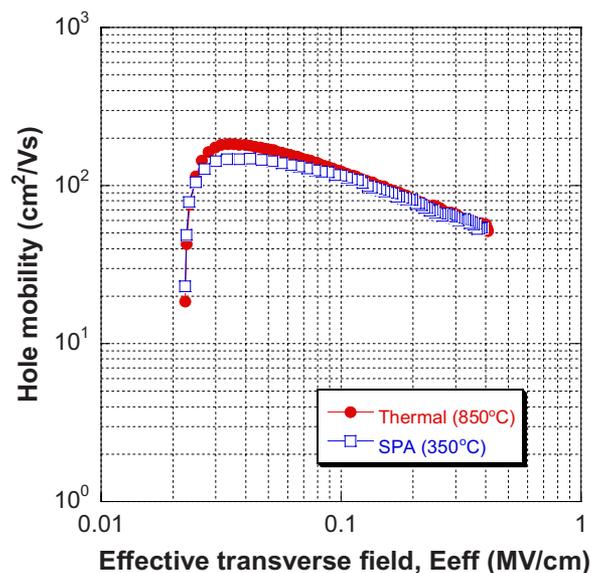


Figure 13. (Color online) Effective mobility as a function of effective transverse field for the Si transistor with poly-Ge gate electrode, PtSi S/D, and SPA gate oxide (350°C) or thermal oxide (850°C).

combining these low temperature processes: (a) I_d - V_g and (b) I_d - V_d characteristics of the Si PMOSFET formed by the fully low temperature transistor technology. To demonstrate a low temperature transistor, we used a 40 mTorr diborane partial pressure in the pretreatment step of the Ge gate electrode growth. The Si PMOSFET shows an excellent I_{on}/I_{off} ratio over 10^7 , low gate leakage, and steep $SS_{min} = 77.9$ mV/dec. Figure 13 shows the effective mobility as a function of the effective transverse field for the Si transistor with a poly-Ge gate electrode, PtSi S/D, and SPA gate oxide (350°C) or thermal oxide (850°C). From an inversion–capacitance measurement at 1 MHz and the drain current at $V_d = -0.05$ V, the estimated hole mobility is ~ 150 $\text{cm}^2/\text{V s}$.

Conclusion

A low temperature chemical vapor deposition germanium growth process on silicon dioxide is developed using a diborane pretreatment below 350°C. A thin boron layer is grown on oxide by a diborane gas precursor, which acts as a seed layer for the germanium deposition. Boron in the germanium film is fully activated at 310°C. A fully low temperature processed transistor fabrication technology has been demonstrated by combining the diborane seed for Ge growth, in situ dopant activation (~ 1 m Ω cm), radical gate oxide,

and Schottky S/D junction, resulting in excellent $I_{\text{on}}/I_{\text{off}} > 10^7$. This demonstrated that low temperature technology is useful for realizing monolithic 3D-ICs.

Acknowledgments

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