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Sidewall epitaxial piezoresistor process and characterisation for in-plane force sensing applications

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Abstract: A selective epitaxial fabrication method to form piezoresistors on the sidewalls of microfabricated cantilevers for in-plane force sensing applications and their preliminary characterisation results is reported. The piezoresistors were made of a doped silicon epitaxial layer using a selective deposition technique by tailoring the process conditions. Silicon oxide was used as a mask, dichlorosilane (DCS) was used as a source gas in a reduced pressure environment and HCl was used to improve selectivity. The authors found that the deposition rates were dependent on the trench widths. The authors further characterised the current–voltage behaviour, noise and sensitivity of these epitaxial sidewall piezoresistors. A typical cantilever had resistance of 0.6 k Ω , $1/f$ coefficient, $\alpha = 8$, sensitivity of 1100 V/N (880 V/m) and resolution of 9.5 nN integrated over the band 10 Hz–10 kHz. Its sensitivity and resolution are comparable to single-crystal ion implanted piezoresistors and better than most polysilicon or diffused piezoresistors.

1 Introduction

In-plane force measurements are important in many engineering and science applications [1, 2]. Several piezoresistive micro-electro-mechanical systems (MEMS) devices have been designed to measure in-plane forces [3–14]. Some of these devices have relied on the oblique-angle ion-implantation technique to form sidewall piezoresistors [3, 4, 10, 12, 14]. However, this technique requires an anneal step to activate the dopants and repair the crystal damage because of the high-energy implantation process, which results in a non-uniform doping profile, a deeper junction depth and a decrease in sensitivity. An alternative method to form piezoresistors without the need of a post-doping anneal step is to grow a doped epitaxial layer on the surface of interest. Piezoresistors formed on top of the substrate surface using a doped epitaxial layer have been demonstrated in cantilevers for out-of-plane force sensing [15, 16].

In this study, the authors present a novel fabrication technique to form piezoresistors on the sidewall of cantilever force sensors for in-plane force sensing

applications. Here the authors expand on earlier work with updated details [17]. The resulting piezoresistors on both sidewalls of the cantilevers should form a half-bridge configuration when a conducting metal line along the top surface makes contact with the junction of the two sidewall piezoresistors (Fig. 1). The authors create sidewall piezoresistors by using a recipe to selectively deposit a doped single-crystal silicon epitaxial layer on the sidewalls of cantilevered structures. The authors achieve selective deposition of epitaxial silicon by tailoring the deposition conditions [18–22]. For example, silicon oxide acts as a growth mask, whereas dichlorosilane (DCS) source gas, in a reduced pressure environment with HCl, improves selectivity.

The fabrication process (Fig. 2) started with a 4 in. (100) p-doped (boron) silicon-on-insulator wafer with a device layer resistivity of 3.3 Ω cm. The piezoresistors were n-type (phosphorous doped) to achieve the highest longitudinal piezoresistive coefficient, π_l , in the (100) direction [23]. The wafers were cleaned using a ‘piranha’ solution (90%

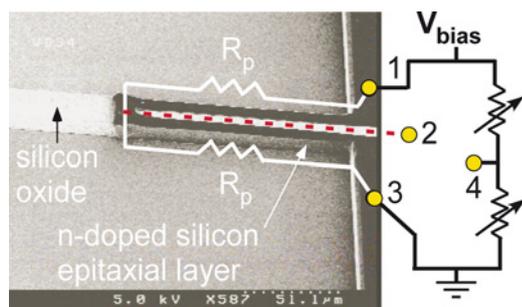


Figure 1 Scanning electron microscopy (SEM) image of sidewall epitaxial piezoresistors on an unreleased cantilever using a selective deposition process

Two piezoresistors on the sidewalls (R_p) form a half-bridge configuration if a metal line is placed along line 2. Dimensions of the piezoresistors on this cantilever are $500 \mu\text{m}$ (L) \times $20 \mu\text{m}$ (W) \times and $2 \mu\text{m}$ (T)

H_2SO_4 and 10% H_2O_2). Alignment marks were then patterned onto the wafers using an isotropic silicon plasma etch process. The device layer (10–20 μm) was etched using a deep reactive ion etch (DRIE) process to define the geometry of the cantilever. The wafers were wet oxidised at 1100°C for 36 min, resulting in $\sim 3700 \text{ \AA}$ of thermal oxide. The resulting oxide was patterned and etched using a buffered oxide etch (BOE: 34% NH_4F , 7% HF and 59% H_2O) to expose silicon (the cantilevers sidewalls) where the piezoresistors would be formed. The remaining oxide masked the subsequent selectively doped epitaxial deposition. An n-type epitaxial layer (phosphorous doped) with a concentration of $1 \times 10^{19} \text{ cm}^{-3}$ was deposited at 980°C and 30 Torr for 8 min, resulting in a doped single-crystal silicon layer with an average thickness of $\sim 2 \mu\text{m}$ with a resistivity of $\sim 0.005 \Omega \text{ cm}$. Table 1 shows the gas

Table 1 Gas flows during the selective epitaxial deposition step

Gas	Flow rate (sccm)
HCl	500
SiH_2Cl_2 (DCS)	400
PH_3	60

SiH_2Cl_2 (DCS) was used as the silicon source, PH_3 was used as the n-type dopant source and HCl was used to improve deposition selectivity

flows during the selective epitaxial deposition step. Metal (99% Al and 1% Si) was then sputtered (1 μm) and patterned using aluminium etch (72% H_3PO_4 , 3% CH_3COOH , 3% HNO_3 and 12% H_2O) to form electrical interconnects. Next, photoresist (1.6 μm thick) was spun and patterned using the same mask that defined the cantilever geometry to protect the metal and oxide layers on the top surface of the cantilevers during the final release. The wafers were diced and each die was then released by etching the buried oxide layer using BOE for 150 min. The photoresist was then removed from each die using a sequence of acetone, methanol and iso-propanol. Finally, each die was dried using critical point drying.

Owing to poor step coverage and significant non-uniformity in the photoresist over the topography during oxide and metal patterning (Fig. 3), the central aluminium interconnect on top of the cantilevers was etched away. Without this central metal line, the half-bridge is removed and bending strain signal from both sidewall piezoresistors cancels out. The authors overcame this problem by depositing a platinum

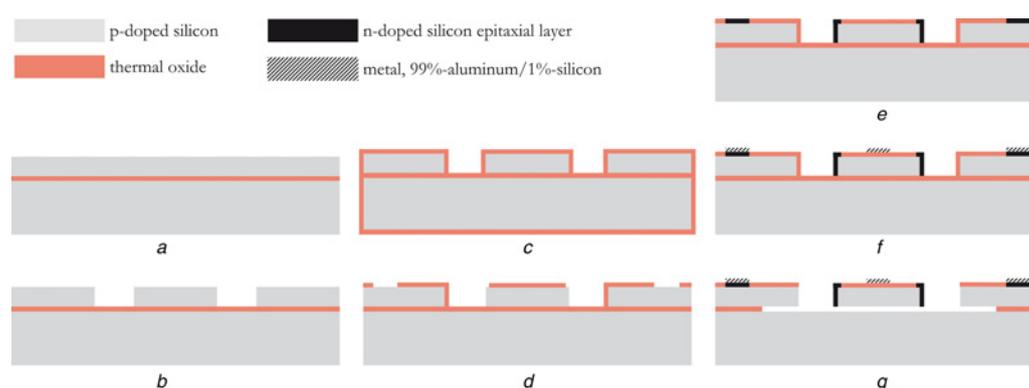


Figure 2 The fabrication process

- Boron-doped double-polished (100) silicon-on-insulator wafer
 - Geometry of the cantilevers was defined by etching the device layer of the wafers using a DRIE process
 - Wafers were wet oxidised
 - Resulting oxide was patterned and etched to expose silicon (cantilevers sidewalls) where piezoresistors would be formed
 - Selective epitaxial deposition of phosphorous-doped layer
 - Metal was then sputtered and patterned to form electrical interconnects
 - Photoresist (1.6 μm thick) was spun and patterned using the same mask used in step (b) to protect the metal and oxide layers on the top surface of the cantilevers during the final release
- Finally, wafers were diced and released by etching the buried oxide layer

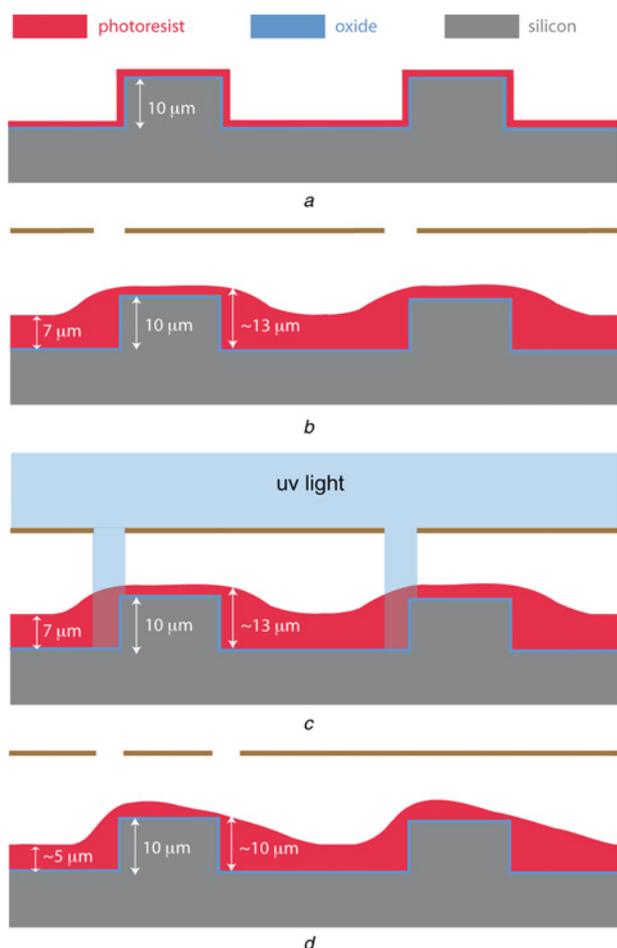


Figure 3 Problems encountered during the patterning of sidewall silicon oxide and aluminium because of poor step coverage and significant non-uniformity in the photoresist over topography

a An ideal step coverage

b In reality, photoresist thickness varied across topography

c An extra exposure time was needed to ensure photoresist covering on the walls was completely exposed and developed away. This resulted in excessive exposure of thinner photoresist on the top surface of the topography, loss of photoresist protection on this area during the oxide etch step, and deposition of epitaxial layer on the exposed silicon

d At the edge of the wafer, photoresist non-uniformity was more significant because of a higher centripetal force during photoresist spinning than that in the centre of the wafer. These problems caused difficulty to pattern and keep the central aluminium interconnect on top of the cantilevers. The aluminium interconnects were fully etched away in the process. The authors overcame this problem by depositing a platinum interconnect (0.25 μm thick) using FIB along the top of one sidewall piezoresistor

interconnect (0.25 μm thick) using focused ion beam (FIB) along the top of one sidewall piezoresistor. This allowed the authors to obtain preliminary performance data from one sidewall piezoresistor and verify its performance alone. Fig. 4 shows a scanning electron microscope (SEM) image of the released cantilever with FIB platinum.

Test structures were included to study trench width effects on the deposition rate of the epitaxial silicon layer. These data

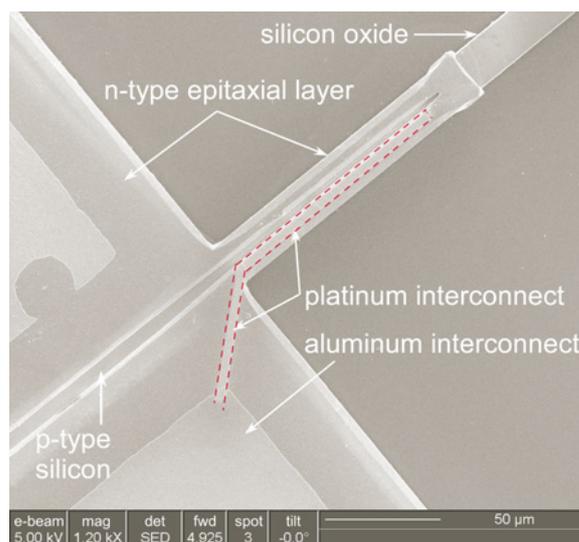


Figure 4 SEM image of the released cantilever with sidewall piezoresistors with platinum interconnect

Width (10–20 μm), thickness (10–20 μm) and length (1000–2000 μm) of the cantilevers were varied. The metal line at the centre was completely etched away. A 0.25 μm thick platinum metal line (shown by the dashed line) was placed on the top of one of the sidewall piezoresistors to avoid cancellation of signals from both piezoresistors

are useful for applications where the width of the trenches is limited by either space or hard stop requirements, such as in shear stress sensors [12, 14] and accelerometers [4, 10]. The thickness of the epitaxial layer deposited on the sidewall of trenches with varying widths (5–500 μm) was measured in the SEM. The authors found that the deposition rate decreases as trench width increases (Fig. 5). This effect may be caused by temperature non-uniformity of exposed silicon surfaces during the deposition process. The silicon surface temperature in the smaller gaps is likely to be higher than that of the larger ones, thus enhancing the deposition rate [20]. Zhang *et al.* [21] reported that the

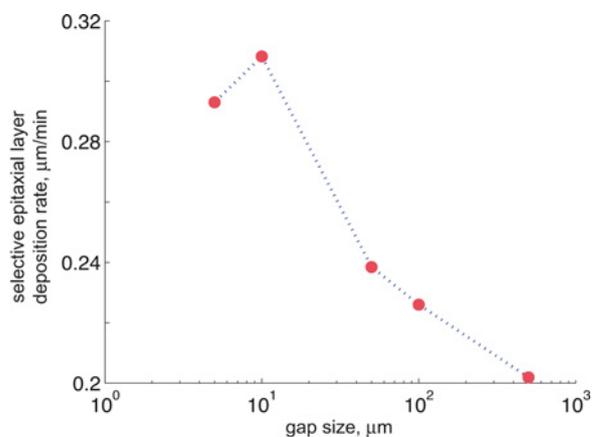


Figure 5 Deposition rate as a function of gap size

The deposition was done at 980°C and 30 Torr for 8 min. The thickness of the epitaxial layer deposited on the sidewall of trenches was measured using SEM

deposition rate is independent of the trench size in smaller trenches, from 2.5 to 20 μm .

The electrical characteristics of a piezoresistor are shown in Fig. 6. Piezoresistor noise is typically dominated by Hooge ($1/f$) noise, $V_{1/f}$ [24–26] and Johnson noise, V_j [27]

$$V_{1/f} = V_b \sqrt{\frac{\alpha}{N\Delta f}} \quad (1)$$

$$V_j = \sqrt{4k_B RT\Delta f} \quad (2)$$

where V_b is the bias voltage applied across the piezoresistor, α is an indicator of piezoresistor quality, N is the total number of carriers in the resistor volume, Δf is the measurement bandwidth, k_B is the Boltzmann constant (1.38×10^{-23} J/K), R is the resistance of the piezoresistor and T is the absolute temperature of the piezoresistor. In this study the noise is higher than predicted and the $1/f$ coefficient, α , is found to be 8 for one of the piezoresistors. This may be because of interface effects of the platinum, aluminium and the silicon epitaxial layers. This hypothesis is supported by the low-frequency noise characteristics, described as $1/f^n$, where $n > 1$ ($n = 1.6$ in our case) suggests constriction resistances and current crowding [28]. More noise measurements are needed to verify the result and test this hypothesis. The authors measured the I – V characteristics of the piezoresistor using an Agilent 4156B and extracted a resistance of ~ 0.6 k Ω with good linearity over -5 to 5 V. This value is slightly lower than the predicted resistance of 0.625 k Ω .

The sensitivities of the cantilevers were characterised using previously reported laser Doppler vibrometer (LDV)

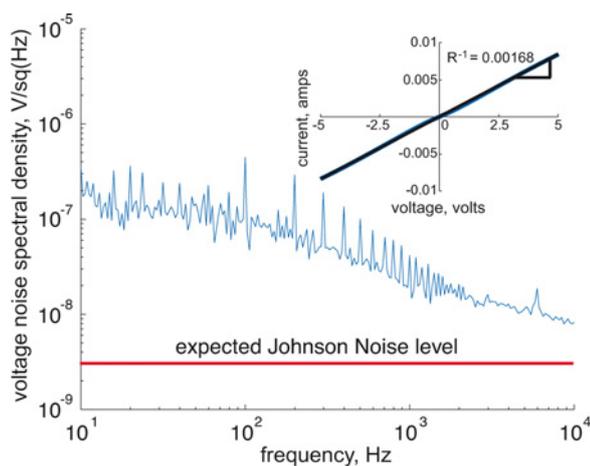


Figure 6 Noise spectrum of a 0.6 k Ω sidewall epitaxial piezoresistor with platinum measured using HP3562A dynamic signal analyser and a bias voltage of 0.1 V

The higher than expected noise level might be because of the imperfect contact between the conductors. Inset: the corresponding I – V curve, measured using Agilent 4156B precision semiconductor parameter analyser, showed ohmic behaviour ($r^2 = 0.9997$) from -5 to 5 V and resistance of ~ 0.6 k Ω

techniques [29, 30]. Three cantilevers with different ratios of piezoresistor to cantilever length (L_p/L_c) were tested. A 1/4-bridge configuration Wheatstone bridge converts piezoresistance change with strain to a voltage using one piezoresistor as a sensing element. This voltage is further amplified with $1000\times$ gain using an AD622 instrumentation amplifier. The cantilevers and a gold-plated surface mount board were glued to a glass slide and mounted on a 90° bracket on a Jodon piezoelectric shaker (Fig. 7). The laser head was positioned above the bracket setup; the laser was directed at the sidewall tip of the cantilever. Initially, the shaker was driven with white noise signal using the source of an HP89441A vector signal analyser; the output from the vibrometer (Polytec OFV-534 Compact Sensor Head) was analysed by the HP89441A to determine a fundamental resonance, $\omega_0 = 8.92$ kHz. The shaker was then driven with a sinusoidal signal at ω_0 and the response from the vibrometer and Wheatstone bridge output was captured by an HP54542A oscilloscope. The tip displacement is determined by integrating the velocity output of the LDV controller (scale 10 mm/s/V), the tip displacement is determined by integrating the output signal. Tip displacement may be converted to force by multiplication with the predicted spring constant to estimate force sensitivity. A typical device exhibits displacement sensitivity of 880 V/m, force sensitivity of 1100 V/N and resolution of 9.5 nN integrated over the band 10 Hz–10 kHz. This is comparable to single-crystal ion implanted piezoresistors and better than most polysilicon or diffused piezoresistors.

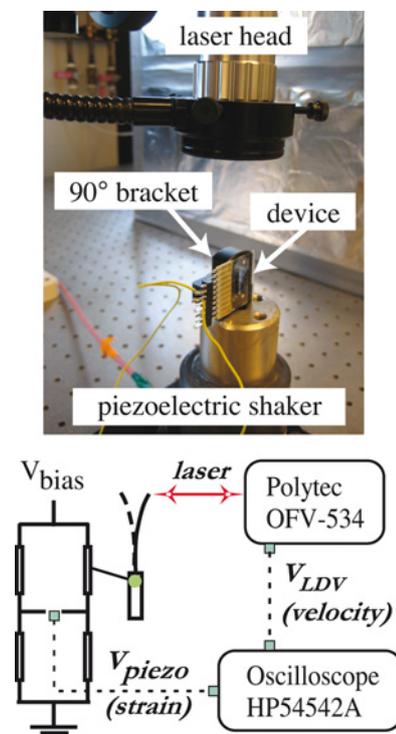


Figure 7 (top) Cantilever was mounted on a 90° bracket on a Jodon piezoelectric shaker (bottom) Schematic of the experimental setup to measure sensitivity

The average bending stress, σ_{avg} , experienced by the piezoresistor was calculated by integrating the bending stress at all points on the piezoresistor along its length and thickness, as shown by

$$\begin{aligned}\sigma_{\text{avg}} &= \frac{F/I \int_{T/2-t_j}^{T/2} y \left(\int_{L_c-L_p}^{L_c} l dl \right) dy}{\int_{T/2-t_j}^{T/2} dy \int_{L_c-L_p}^{L_c} dl} \\ &= \frac{F}{4I} (2L_c - L_p)(T - t_j)\end{aligned}\quad (3)$$

where I is the area moment of inertia of the cantilever ($I = TW^3/12$), T and W are the thickness and the width of the cantilever, respectively, t_j is the junction depth or the thickness of the piezoresistor, L_c is the length of the cantilever and L_p is the length of the piezoresistor. The experimental longitudinal piezoresistive coefficients, $\pi_{1,\text{exp}}$, are estimated by

$$\pi_{1,\text{exp}} = \frac{\Delta R/R}{\sigma_{\text{avg}}} = \frac{4V_{\text{out}}/V_b}{3F/TW^3(2L_c - L_p)(T - t_j)} \quad (4)$$

where $\Delta R/R$ is the relative change of the resistance of the piezoresistor, V_{out} and V_b are the output and bias voltage of the Wheatstone 1/4-bridge, and F is the in-plane force applied to the tip of the cantilever. Finally, the experimental piezoresistive coefficients as a function of dopant concentration at room temperature, $P(N)$, were calculated using

$$P(N) = \frac{\pi_{1,\text{exp}}}{\pi_{1,\text{max}}} \quad (5)$$

where $\pi_{1,\text{max}}$ for phosphorus was predicted by Kanda to be $102 \times 10^{-11} \text{ Pa}^{-1}$ [23]. The $P(N)$ values from this work were then plotted against the results from other researchers [16, 31], as well as the theoretical prediction by Kanda [23] (Fig. 8). Uncertainties are attributed mainly to variations in the dimensions of the cantilevers (approximately 20% variability of W and T) and the piezoresistors (approximately 10% variability in t_j).

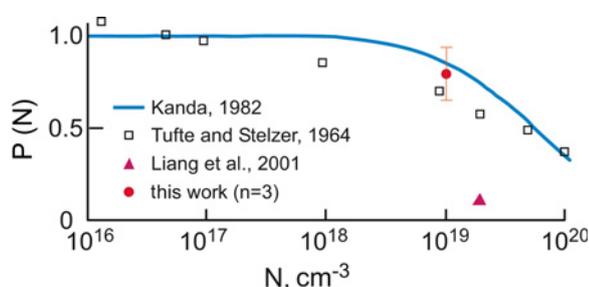


Figure 8 Values of experimental $P(N)$ from this work and other researchers [16, 31], as well as the theoretical prediction by Kanda [23]

The average $P(N)$ from this work ($n = 3$) was 0.79 with a standard deviation of 0.14

2 Conclusion

To conclude, the authors have demonstrated a promising fabrication technique to form piezoresistors on the sidewalls of microstructures for in-plane force sensing applications and early findings on their electromechanical characteristics. A typical cantilever had resistance of 0.6 k Ω , $1/f$ coefficient, $\alpha = 8$, sensitivity of 1100 V/N (880 V/m) and resolution of 9.5 nN integrated over the band 10 Hz–10 kHz. Its sensitivity and resolution are comparable to single-crystal ion implanted piezoresistors and better than most polysilicon or diffused piezoresistors. Future work will focus on: improving the fabrication process to achieve more robust interconnect (without FIB metal), introducing different dopant concentrations to characterise performance over a range of parameters, further noise characterisation and study, and improving experimental setups for sensitivity and noise measurements.

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