

High Aspect Ratio Si Etching in STS2

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I. INTRODUCTION

Deep reactive ion etching (DRIE) is one of the most important etching techniques because it is independent of crystal orientation and does not require any wet process. DRIE can be applied for many applications. For examples, this technique can be used to fabricate MEMS devices (e.g. accelerometers, scanners, etc.), microfluidic devices, electrical through wafer interconnects, and so on. In many cases, when DRIE can achieve high aspect ratio (AR) silicon etching, device design flexibility can be increased and device performance also can be improved. Therefore, it is important to have high AR etching recipes.

In this paper, I discuss the background for high AR process, and introduce three different recipes that have been developed for use in STS2: (1) HAR recipe, (2) low frequency bias recipe, and (3) low power recipe. HAR recipe is developed to achieve the AR over 40 for 2 μ m-wide trenches. The low frequency bias recipe is to enable relatively high AR with small notching effect in SOI wafer process. Finally, the low power recipe is to minimize the heating problem that is caused during DRIE.

II. BACKGROUND FOR HIGH AR PROCESS

For high AR etching, it is important to control the lateral etch rate and to enhance the vertical etch rate. Ideally, the vertical ion bombardment energy have to be high enough to achieve the desired vertical etch rate, while the lateral bombardment should be weak enough, not to make lateral etching by etch-through of the passivation layer. These vertical and lateral etch rates can be adjusted to achieve high AR etching by varying several parameters such as gas flow, coil power, EM current, etc.

Table 1 is a summary of the general process trends in DRIE. The trends indicated in this table will be accurate in most cases but not all because of the dependency on wafer pattern, exposed area, and applications.

Table1. Summary of process trends.

Trends for Controlling process results	Etch rate	Profile (↑ negative) (↓ positive)	Selectivity	Grass	Breakdown	Sidewall Roughness
Etch gas increase	↑↑	↑↑	↑	↓	↑	↓
Dep gas increase	↓↔	↔	↑	↑	↓↔	↓
Etch:Dep time ratio increase	↑	↑	↑↔	↑	↑↔	↑
Pressure increase	↑↑	↑	↑	↓↔	↑	↑
Dep Coil Power increase	↓↔	↓↔	↑↔	↑	↓↔	↓
Etch Coil Power increase	↑	↑	↑	↓	↑	↑
Platen Power increase	↑↔	↑↔	↓	↓	↔	↔
EM1 value (e) increase	↓↔	↓↔	↑	↑↔	↓↔	↔
EM1 delay (e) increase	↑↔	↑↔	↓	↓↔	↑↔	↔

E=etch
 ↔ no effect or negligible effect
 ↑ increase
 ↓ decrease

Information in Table 1 can be used to control etch profiles. Based on this process information, high AR recipes have been developed, which can be used in STS2.

III. RECIPE DEVELOPMENT

A. HAR

“HAR” is one of recipes that are provided by STS2, in order to give users the starting point for recipe development. To optimize this recipe, DRIE characteristics were investigated by varying several process conditions.

A.1. Influence of Electromagnetic (EM) Current

EM flux generated in the chamber is a critical factor that affects ion bombardments at a sample wafer. Decreasing EM flux makes the incident ions more directional toward the wafer, thus increasing the number of ions arriving at the bottom of trenches. As a result, grass is reduced at a cost of degraded profile verticality. The following plot (Fig. 1) demonstrates trade-off between grass and verticality, which is influenced by the EM current.

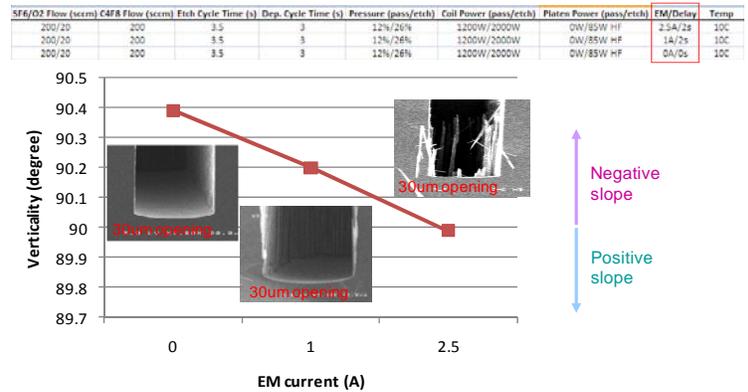


Fig. 1. Verticality and grass vs. EM current

Lots of grasses are observed in the trench at EM current of 2.5A, but the grasses are significantly reduced by decreasing the EM current. However, its side-effect is that the initially vertical sidewall at 2.5A bias becomes negative-angled due to the increased ion bombardment at the base of the trench.

A.2. Influence of Coil Power

Higher coil power increases plasma density, therefore resulting in increased etch rate, reentrant profile, and reduced grass. Figure 2 shows the influence of varying the etch coil power. When the coil power is increased from 2000W to 2400W, the sidewall slope becomes negative because of higher

etch rate. Although grass is reduced with the increased coil power, the variation of coil power does not have large impact on reducing grass.

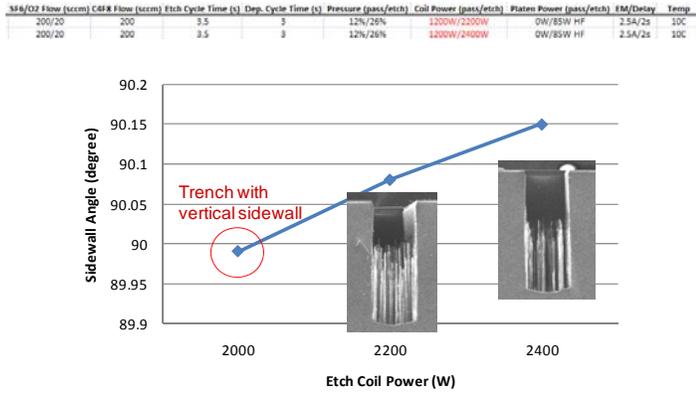


Fig. 2. Sidewall angle and grass vs. Etch coil power

A.3. Influence of Bias (Platen) Power

The bias power (or platen power) removes deposition from the base of the trench mainly as a result of ion-assisted bombardment during the etch step. Thus, the bias power affects the profile. When the platen power increases, the number of ions reaching the base becomes larger and this gives rise to negative angled sidewall and less or no grass. This is demonstrated in Fig. 3. The effect of the bias power is very similar to that of the coil power, but from Fig. 2 and Fig. 3, we can see that the bias power is a more critical factor than the coil power in terms of controlling grass.

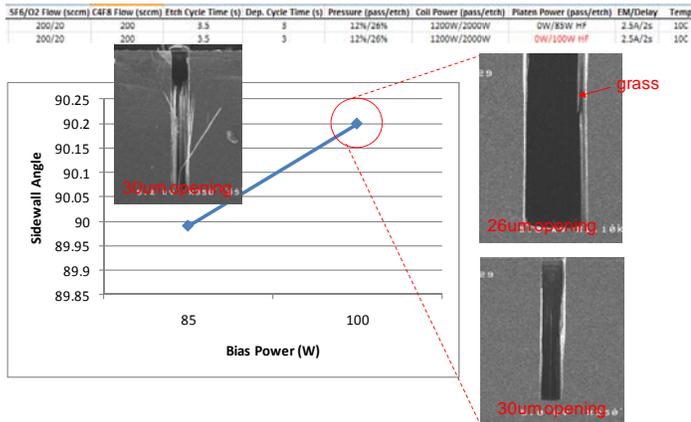


Fig. 3. Sidewall angle and grass vs. Bias power

A.4. Influence of Temperature

The deposition step is strongly dependent on temperature. As the temperature decreases, the deposition rate increases. This effect may cause grassing. Therefore, higher temperature is preferred for the removal of grass [1].

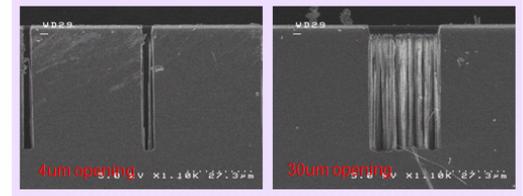
In our experiment, however, the opposite phenomenon was observed (Table 2). As the temperature increased, the profile became reentrant as expected [1], but more grasses were grown in trenches. Grass that used to form over 12μm-wide trenches at

10°C, started to appear from 4μm-wide trenches at 20°C. This may be resulted from the temperature control problem of the central system. For further investigation, we will need to measure the actual temperature of the wafer during operation.

Table 2. Influence of temperature on profiles

SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	Pressure (pass/etch)	Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay	Temp
200/20	200	3.5	3	12%/26%	1200W/2000W	0W/85W HF	2.5A/2s	10C
200/20	200	3.5	3	12%/26%	1200W/2000W	0W/85W HF	2.5A/2s	20C

10°C	20°C
<ul style="list-style-type: none"> Grass starts to appear from 12-14 μm-wide trench Sidewall angle ~ 90° 	<ul style="list-style-type: none"> Grass starts to appear from 4μm-wide trench Sidewall angle ~ 90.2°



A. 5. Optimized HAR Recipe

Based on the results from the section A.1 to A.4, HAR recipe has been optimized to provide high AR etching with vertical profiles. The following table shows the detailed setting of the optimized HAR recipe.

Table 3. Optimized HAR recipe

SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)
200/20	200	3.5	3
Pressure (pass/etch)	Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay
12%/26%	1200W/2000W	0W/85W HF	2.5A/2s

Figure 4 shows the trench profiles obtained after 550 cycle runs. From three samples, the average AR for 2μm-wide trenches is 41.7 with standard deviation of 0.28. The profile is almost perfectly vertical (verticality of 89.99°), and its sidewall roughness and undercut are ~150nm and ~350nm, respectively.

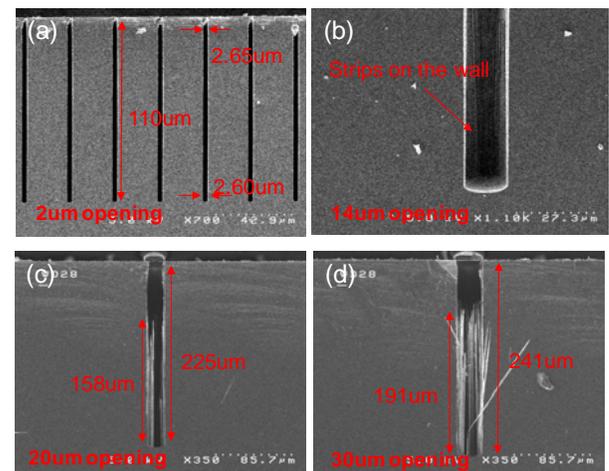


Fig. 4. HAR etching profile after 550 cycles run. (a) 2μm-wide trench, (b) 14μm-wide trench, (c) 20μm-wide trench, (d) 30μm-wide trench.

The only problem of this optimized recipe is grass. Grass starts to appear in trenches wider than 12 μm (Fig. 5). Therefore, this HAR recipe will be most suitable for creating high AR patterns with feature size smaller than 12 μm .

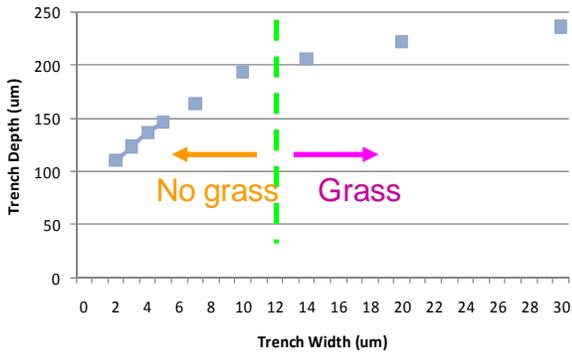


Fig. 5. Plot of aspect ratio dependent etching profile with grass information.

B. LOW FREQUENCY BIAS RECIPE

Low frequency (LF) bias recipe has been developed to achieve small notching and relatively high AR for SOI wafer processing. The detailed setting of this recipe is shown in Table 4. The reason to use LF bias in this recipe is to minimize notching. Notching is a common phenomenon in time-multiplexed etch processes, which is caused by charge accumulation [2]. This phenomenon produces a lateral etch on the interface between silicon and the underlying dielectric layer. LF bias RF power pulsing reduces ionic charging of the oxide layer beneath the silicon by allowing charge to dissipate during the “off” cycle. Therefore, LF bias can control the notching.

Table 4. Low frequency bias recipe

SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	
450/45	100	3	2	
Pressure (pass/etch)	Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay	Temp
15%/15%	1000W/2400W	0W/45W	0A/0s	10C

Figure 6 shows the etch result of this LF bias recipe. The etch rate for 4 μm -gap trench is $\sim 6\mu\text{m}/\text{min}$, and the selectivity between silicon and oxide is 420:1. The undercut under the oxide mask is 0.5 μm as shown in the figure. Up to 51 μm , the profile is very vertical, showing the sidewall angle of 89.97°. In addition, no grass was found in large trench (1.8mm X 1.8mm) up to 300 μm depth.

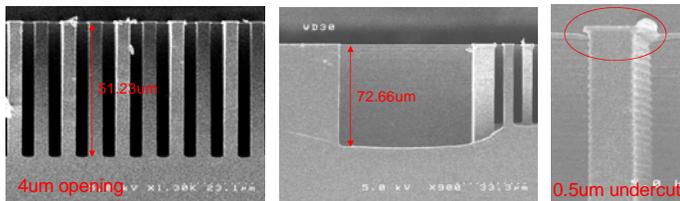


Fig. 6. SEM images of LF bias recipe etching profile.

Notching characteristic was also investigated by overetching silicon by 20%. This resulted in 0.5 μm notching as

shown in Fig. 7. In the left image, we can see that some of trench structures are tilted and misaligned. This happened due to the force applied while cleaving.

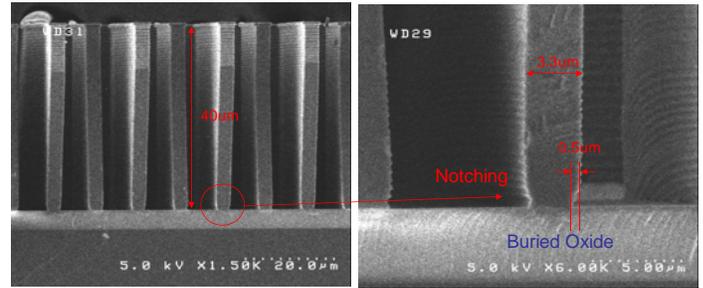


Fig. 7. SEM images that show notching in a SOI wafer

Because of the vertical profile, small notching effect, and high selectivity, the LF bias recipe can be used to fabricate various MEMS devices.

C. LOW POWER RECIPE

Low power recipe has been developed to solve the heating problem that is caused during DRIE. High power ion bombardments that are occurred during DRIE generate lots of heat in device structures. If the structures are connected each other with large contact area, heat will be easily dissipated. However, if it is a suspended membrane structure like a micromirror (Fig. 8) and held by a thin and long springs, the silicon springs may be burned by heating due to its high thermal resistance. Figure 9 shows the result of silicon burning that happened during the fabrication of MEMS scanners. Because of the heating problem during the etching, springs were disconnected and comb-fingers connected to the suspended structures were burned and disappeared. All other thin structures that are connected with the substrate remained intact.

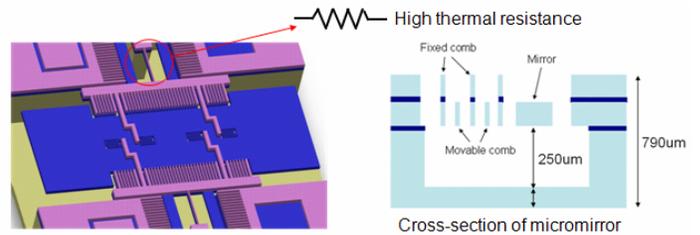


Fig. 8. Schematic of micromirror structure that were tried to fabricate.

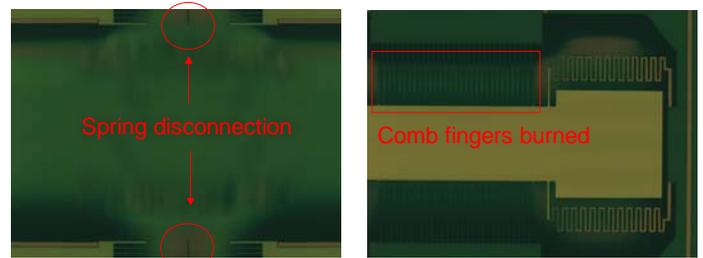


Fig. 9. Structure disconnection and burning due to the heating caused during DRIE

To solve this problem, I have developed a low power recipe as shown in Table 5. This is basically the LF bias recipe in section B, but the etch coil power has been decreased to 1500W to minimize the heating.

Table 5. Low power recipe

SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	Pressure (pass/etch)
450/45	100	3	2	15%/15%
Coil Power (pass/etch)	Platen Power (pass/etch)	EM/Delay	Temp	
1000W/1500W	0W/45W	0A/0s	10C	

The following trenches (Fig. 10) were created by using the low power recipe. For 4 μ m-wide trenches, the etch rate is 4.89 μ m/min and the selectivity between silicon and oxide is 580:1. The sidewall angle of the profile was 89.93 $^\circ$.

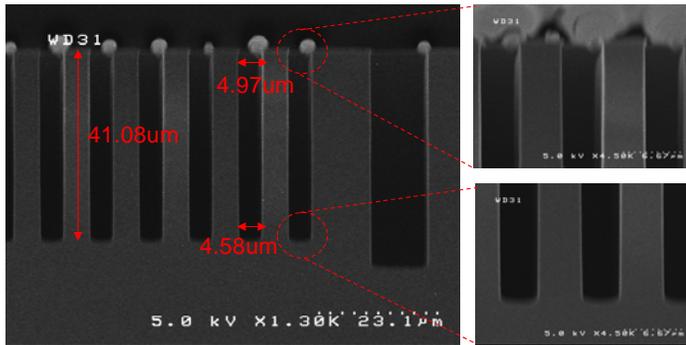


Fig. 10. SEM images of low power recipe etching profile

This low power recipe was applied to fabricate MEMS scanners. Our strategy to solve the heating problem during DRIE was using two step etching. As shown in Fig. 11, we first etched the top device layer using the LF bias recipe described in section B, and then released the micromirror structure by etching the bottom device layer using the low power recipe. For the top device layer etching, we did not need low temperature process because the bottom device layer provides large heat conduction paths. To be cautious, the wafer was cooled down twice during the low power DRIE of the bottom layer.

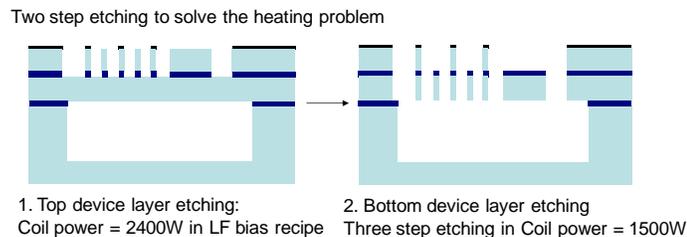


Fig. 11. Fabrication strategy to minimize the heating problem in DRIE for the fabrication of MEMS scanners.

Using this strategy, MEMS scanners (Fig. 12) were successfully fabricated. Thin and long springs that are connected to the suspended micromirror were preserved during DRIE. In addition, 4 μ m-gap comb-finger profiles were very vertical and nicely aligned. From this result, it is shown that the low power recipe does work to solve the DRIE heating problem. Therefore,

this recipe will be beneficial for fabricating membrane structures.

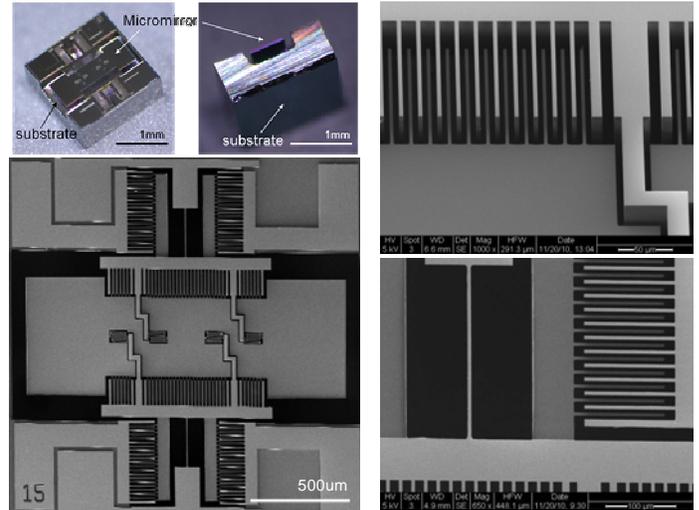


Fig. 12. SEM images of fabricated MEMS scanner

IV. CONCLUSION

Three kinds of recipes have been developed for high AR etching: (1) HAR, (2) LF bias recipe, and (3) low power recipe. HAR achieves AR over 40 for 2 μ m-gap trenches. Since grass exists in trenches wider than 12 μ m, this recipe will be most suitable for creating high AR patterns smaller than 12 μ m. LF bias recipe is for use in SOI wafer process. It shows small notching (0.5 μ m) at the interface of silicon and oxide, and creates relatively high aspect ratio trenches. Finally, low power recipe has been made to minimize heating problem during DRIE. We believe these three recipes will greatly facilitate fabrication of MEMS devices by providing more flexibility for both device and process designs.

ACKNOWLEDGEMENT

I would like to thank Dr. James McVittie for fruitful discussion and dedicated support.

REFERENCES

- [1] S. B. Jo, M. W. Lee, S. G. Lee, E. H. Lee, S. G. Park, and B. H. O, "Characterization of a modified Bosch-type process for silicon mold fabrication," *J. Vac. Sci. Technol. A* 23, 905, June, 2005.
- [2] J. Tian and M. Bartek, "Simultaneous through-silicon via and large cavity formation using deep reactive ion etching and aluminum etch-stop layer," Proceedings on Electronics Components and Technology Conference, Lake Buena Vista, FL, USA, pp. 1787 – 1792, May 2008.